In the Claims:

Claim 1 (original): A cascode amplifier circuit, said cascode amplifier circuit being connected to a target memory cell via a bit line during a read operation involving said target memory cell, said cascode amplifier circuit comprising:

a first intrinsic FET having a source connected to said bit line and a drain connected to a first node, a bit line voltage being generated at said source of said first intrinsic FET, a sense amp input voltage being generated at said first node;

a second intrinsic FET having a gate connected to said source of said first intrinsic FET and a source connected to a reference voltage, said second intrinsic FET having a drain connected at a second node to a gate of said first intrinsic FET;

a third intrinsic FET having a source connected to said first node and a gate connected to a supply voltage, said third intrinsic FET further providing a load across said supply voltage and said first node;

a fourth FET having a source connected to said second node and a drain connected to said supply voltage, said fourth FET having a gate connected to an input control voltage.

Claim 2 (original): The cascode amplifier circuit of claim 1, wherein said second intrinsic FET operates in the saturation region.

Claim 3 (original): The cascode amplifier circuit of claim 1, wherein said second intrinsic FET has a gate width to gate length ratio of approximately 6/0.9.

Claim 4 (canceled)

Claim 5 (original): The cascode amplifier circuit of claim 1, wherein said reference voltage is ground.

Claim 6 (original): The cascode amplifier circuit of claim 1, wherein said target memory cell is capable of storing two binary bits.

Claim 7 (original): The cascode amplifier circuit of claim 1, wherein said third intrinsic FET has a drain connected to said supply voltage through a first enable transistor, said fourth FET having a drain connected to said supply voltage through a second enable transistor.

Claim 8 (original): A cascode amplifier circuit, said cascode amplifier circuit being connected to a target memory cell via a bit line during a read operation involving said target memory cell, said cascode amplifier circuit comprising:

means for receiving an input control voltage comprising an NFET, said NFET having a drain connected to a supply voltage and a gate connected to said input control voltage;

means for generating a bit line voltage responsive to said control voltage comprising a first intrinsic FET, said first intrinsic FET having a source connected to said bit line and a drain connected to a first node, said bit line voltage being generated at said source of said first intrinsic FET, a sense amp input voltage being generated at said first node;

means for generating a negative feedback voltage at a second node responsive to said bit line voltage comprising a second intrinsic FET, said second intrinsic FET having a gate connected to said source of said first intrinsic FET and a source connected to a reference voltage, said second intrinsic FET having a drain connected at said second node to a gate of said first intrinsic FET and to a source of said NFET;

means for generating a load across said supply voltage and said first node comprising a third intrinsic FET, said third intrinsic FET having a source connected to said first node and a gate connected to said supply voltage.

Claim 9 (original): The cascode amplifier circuit of claim 8, wherein said second intrinsic FET operates in the saturation region.

Claim 10 (original): The cascode amplifier circuit of claim 8, wherein said intrinsic FET means has a gate width to gate length ratio of approximately 6/0.9.

Claim 11 (original): The cascode amplifier circuit of claim 8, wherein said reference voltage is ground.

Claim 12 (original): The cascode amplifier circuit of claim 8, wherein said target memory cell is capable of storing two binary bits.

Claim 13 (original): The cascode amplifier circuit of claim 8, wherein said third intrinsic FET has a drain connected to said supply voltage through a first enable transistor, said NFET having a drain connected to said supply voltage through a second enable transistor.

Claim 14 (original): A cascode amplifier circuit, said cascode amplifier circuit being connected to a target memory cell via a bit line during a read operation involving said target memory cell, said cascode amplifier circuit including a first intrinsic FET having a source connected to said bit line and a drain connected to a first node, a bit line voltage being generated at said source of said first intrinsic FET, a sense amp input voltage being generated at said first node, said cascode amplifier circuit being characterized by:

a second intrinsic FET having a gate connected to said source of said first intrinsic FET and a source connected to a reference voltage, said second intrinsic FET having a drain connected at a second node to a gate of said first intrinsic FET; a third intrinsic FET having a source connected to said first node and a gate connected to a supply voltage, said third intrinsic FET further providing a load across said supply voltage and said first node; a fourth FET having a source connected to said second node and a drain connected to said supply voltage, said fourth FET having a gate connected to an input control voltage.

Claim 15 (original): The cascode amplifier circuit of claim 14, wherein said second intrinsic FET operates in the saturation region.

Claim 16 (original): The cascode amplifier circuit of claim 14, wherein said second intrinsic FET has a gate width to gate length ratio of approximately 6/0.9.

Claim 17 (original): The cascode amplifier circuit of claim 14, wherein said bit line voltage corresponds to said input control voltage.

Claim 18 (original): The cascode amplifier circuit of claim 14, wherein said reference voltage is ground.

Claim 19 (original): The cascode amplifier circuit of claim 14, wherein said target memory cell is capable of storing two binary bits.

Claim 20 (original): The cascode amplifier circuit of claim 14, wherein said third intrinsic FET has a drain connected to said supply voltage through a first enable transistor, said fourth FET having a drain connected to said supply voltage through a second enable transistor.